EP 1855 C

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 651 431 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **94307986.3**

(51) Int. Cl.[6] : **H01L 21/20**

(22) Date of filing : **31.10.94**

(30) Priority : **29.10.93 JP 294633/93**
09.11.93 JP 303436/93
12.11.93 JP 307206/93
20.06.94 JP 162705/94

(43) Date of publication of application :
03.05.95 Bulletin 95/18

(84) Designated Contracting States :
DE FR GB NL

(71) Applicant : **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.**
398 Hase
Atsugi-shi Kanagawa-ken, 243 (JP)

(72) Inventor : **Ohtani, Hisashi**
Mac Aikoishida Court,
501 7-896-1, Takamori
Isehara-shi, Kanagawa-ken 259-11 (JP)
Inventor : **Miyanaga, Akiharu**
2-505, 3-4-1, Minamigaoka
Hadano-shi, Kanagawa-ken 257 (JP)
Inventor : **Fukunaga, Takeshi**
Flat SEL-A 105,
304-1, Hase
Atsugi-shi, Kanagawa-ken 243 (JP)
Inventor : **Zhang, Hongyong**
Paresu Miyagami 302,
1-10-15, Fukamidai
Yamato-shi, Kanagawa-ken 243 (JP)

(74) Representative : **Milhench, Howard Leslie et al**
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

(54) Method of crystallizing a silicone layer and semiconductor devices obtained by using the method.

(57) A process for fabricating a highly stable and reliable semiconductor, comprising : coating the surface of an amorphous silicon film with a solution containing a catalyst element capable of accelerating the crystallization of the amorphous silicon film, and heat treating the amorphous silicon film thereafter to crystallize the film.

EP 0 651 431 A2

controlling the amount of the catalyst element to be incorporated in the amorphous silicon film.

SUMMARY OF THE INVENTION

In the light of the aforementioned circumstances, the present invention aims to fabricate with high productivity, a thin film of crystalline silicon semiconductor by a heat treatment at a relatively low temperature using a catalyst element, provided that the catalyst element is incorporated by precisely controlling the quantity thereof.

In accordance with one aspect of the present invention, the foregoing objects can be achieved by providing an amorphous silicon film with a catalytic element for promoting the crystallization thereof or a compound including the catalytic element in contact with the amorphous silicon film, and heat treating the amorphous silicon with said catalytic element or said compound being in contact therewith, thereby, the silicon film is crystallized.

Preferably but not essentially, a solution containing the catalytic element is provided in contact with an amorphous silicon film in order to introduce the catalytic element into the amorphous silicon film.

According to a second aspect of the present invention there is provided a method of manufacturing a semiconductor device comprising addingamaterial selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, Pd, Sn, P, As and Sb into a silicon semiconductor film or a portion thereof at a trace amount by contacting a solution containing said material with the silicon film and then crystallize the silicon semiconductor film by heating at a relatively low temperature.

According to a third aspect of the present invention there is provided a method for manufacturing a semiconductor device comprising the steps of: adding a crystallization promoting material into a first region of a silicon film formed on a surface, by disposing a solution containing said crystallization promoting material in contact with a selected portion of the silicon film; and heating said silicon film in order that crystals grow from said first region toward a second region of the silicon film to which said crystallization promoting material is not directly added.

According to a fourth aspect of the present invention there is provided a method of manufacturing a semiconductor device comprising:preparing a solution containing a compound dissolved or dispersed in a polar or non-polar solvent, the compound including a crystallization promoting material; disposing the solution in contact with a silicon film and crystallizing said silicon film by heating.

The present invention also extends to a semiconductor device having at least an active region comprising crystalline silicon and to a method of manufacturing an insulated gate field effect semiconductor device. Examples of how these devices can be manufactured are described in the following description but it should be noted that the invention is not limited to the methods described therein, i.e. the invention is not limited to providing a catalyst for promoting crystallisation or to providing the catalyst by way of a solution.

Therefore according to a fifth aspect of the present invention there is provided a method for manufacturing an insulated gate field effect semiconductor device comprising the steps of: forming an amorphous silicon film on an insulating surface; crystallizing said silicon film; and oxidizing a surface of said silicon film in an oxidizing atmosphere containing water vapor in order to form a gate insulating film.

In addition, even if a catalyst is used to obtain a semiconductor device having an active region of crystalline silicon, the active region may comprise crystalline silicon which does not contain any catalyst as it has been grown away from its region of seeding. Such a semiconductor device is novel and could still be readily identified by examination of its crystalline planes even if the region which was catalysed subsequently has been removed. Therefore, according to a sixth embodiment of the invention there is provided a semiconductor device including at least an active region comprising crystalline silicon formed on a substrate, wherein a surface of said silicon film has at least one of planes {111}, those expressed by {hkl} (h+k=1), and a neighborhood thereof.

Furthermore, according to a seventh embodiment of the present invention there is provided a method of manufacturing a semiconductor device, said method comprising seeding a first region of a silicon substrate and heating said substrate to grow crystals laterally from said first region to a second region of said silicon substrate.

By utilizing the silicon film having a crystallinity thus formed, it is possible to form an active region including therein at least one electric junction such as PN, PI or NI junction. Examples of semiconductor devices are thin film transistors (TFT), diodes, photo sensor, etc.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing objects and features of the present invention will be described in detail with reference to the attached figures in which:

Figs. 1A to 1D are cross sectional views for forming a crystalline silicon film in accordance with the present invention;

Figs. 2A and 2B are cross sectional views showing a formation of a crystalline silicon film in accordance with the present invention;

Fig. 3 is a graph showing a relation of a lateral growth length of crystals with respect to a concentration of nickel in a solution;

nickel, the solution can be directly formed on the surface of an amorphous silicon film. However, it is possible to interpose between the amorphous silicon film and the solution a material for increasing the adhesivity therebetween, for example, OAP (containing hexamethyl disilazane as a main component, produced by Tokyo Oka Kogyo) which is used to increase adhesivity of a resist.

The concentration of the catalyst element in the solution depends on the kind of the solution, however, roughly speaking, the concentration of the catalyst element such as nickel by weight in the solution is 1 ppm to 200 ppm, and preferably, 1 ppm to 50 ppm, and more preferably 10 ppm or lower. The concentration is determined based on the nickel concentration in the silicon film or the resistance against hydrofluoric acid of the film upon completion of the crystallization.

The crystal growth can be controlled by applying the solution containing the catalyst element to a selected portion of the amorphous silicon film. In particular, the crystals can be grown in the silicon film by heating the silicon film in a direction approximately parallel with the plane of the silicon film from the region onto which the solution is directly applied toward the region onto which the solution is not applied.

It is also confirmed that this lateral growth region contains the catalyst element at a lower concentration. It is useful to utilize a crystalline silicon film as an active layer region for a semiconductor device, however, in general, the concentration of the impurity in the active region is preferably as low as possible. Accordingly, the use of the lateral growth region for the active layer region is useful in device fabrication.

The use of nickel as the catalyst element is particularly effective in the process according to the present invention. However, other useful catalyst elements include nickel (Ni), palladium (Pd), platinum (Pt), copper (Cu), silver (Ag), gold (Au), indium (In), tin (Sn), phosphorus (P), arsenic (As), and antimony (Sb). Otherwise, the catalyst element may be at least one selected from the elements belonging to the Group VIII, IIIb, IVb, and Vb of the periodic table.

EXAMPLE 1

The present example refers to a process for fabricating a crystalline silicon film on the surface of a glass substrate. Referring to Figs. 1A-1D, the process for incorporating a catalyst element (nickel in this case) into the amorphous silicon film is described below. A Corning 7059 glass substrate 100 mm x 100 mm in size is used.

An amorphous silicon film from 100 to 1,500 Å in thickness is deposited by plasma CVD or LPCVD. More specifically in this case, an amorphous silicon film 12 is deposited at a thickness of 1,000 Å by plasma CVD (Fig. 1A).

Then, the amorphous silicon film is subjected to hydrofluoric acid treatment to remove impurities and a natural oxide formed thereon, if necessary. This treatment is followed by the deposition of an oxide film 13 on the amorphous silicon film to a thickness of from 10 to 50 Å. A natural oxide film may be utilized as the oxide film. The precise thickness of the oxide film 13 is not available because the film is extremely thin. However, the natural oxide film is assumably about 20 Å in thickness. The oxide film 13 is deposited by irradiating an ultraviolet (UV) radiation in an oxygen atmosphere for a duration of 5 minutes. The oxide film 13 can be formed otherwise by thermal oxidation. Furthermore, the oxide film can be formed by a treatment using aqueous hydrogen peroxide.

The oxide film 13 is provided with an aim to fully spread the acetate solution containing nickel, which is to be applied in the later step, on the entire surface of the amorphous silicon film. More briefly, the oxide film 13 is provided for improving the wettability of the amorphous silicon film. If the aqueous acetate solution were to be applied directly, for instance, the amorphous silicon film would repel the aqueous acetate solution to prevent nickel from being incorporated uniformly into the surface of the amorphous silicon film.

An aqueous acetate solution containing nickel added therein is prepared thereafter. More specifically, an aqueous acetate solution containing nickel at a concentration of 10 to 200 ppm, e.g. 100 ppm, is prepared. Two milliliters of the resulting acetate solution is dropped to the surface of the oxide film 13 on the amorphous silicon film 12, and is maintained as it is for a predetermined duration of time, preferably for a duration of 0.5 minutes or longer, e.g. for a duration of 5 minutes. Spin drying at 2,000 rpm using a spinner is effected for 60 seconds thereafter to remove the unnecessary solution (Figs. 1C and 1D).

The concentration of nickel in the acetate solution is practically 1 ppm or more, preferably,10 ppm or higher. The solution needs not be only an acetate solution, and other applicable solutions include those of hydrochlorides, nitrates, and sulfates. Otherwise, those of organic octylates and toluene can be used as well. In case of using the organic solutions, the oxide film 13 need not be incorporated because the solution can be directly applied to the amorphous silicon film to introduce the catalyst elements into the film.

The coating of the solution is carried out at one time or may be repeated, thereby, it is possible to form a film containing nickel on the surface of the amorphous silicon film 12 uniformly to a thickness of several angstrom to several hundreds angstrom after the spin dry. The nickel contained in this film will diffuse into the amorphous silicon film during a heating process carried out later and will function to promote the crystallization of the amorphous silicon film. By the way, it is the inventors' intention that the film con-

The datum plotted in Fig. 3 are for the case that the structure was held for a duration of 5 minutes after applying the nickel-containing aqueous acetate solution. However, the distance of crystal growth along the lateral direction changes with the retention time.

In case of using an aqueous acetate solution containing nickel at a concentration of 100 ppm, for instance, longer distance of crystal growth can be obtained with increasing retention time up to 1 minute. However, once a retention time of 1 minute or longer is set, the further increase becomes insignificant.

In case an aqueous acetate solution containing nickel at a concentration of 50 ppm is used, the retention time increases proportional to the distance of the crystal growth along the lateral direction. However, the increment tends to saturate with increasing retention time to 5 minutes or longer.

Furthermore, it should be noted that temperature greatly influences the time necessary for a reaction to achieve an equilibrium. Accordingly, the retention time is also subject to the temperature, and a strict control of the temperature is indispensable. Thus, the distance of crystal growth can be increased in total by elevating the temperature of heat treatment and by elongating the duration of the heat treatment.

Figs. 4 and 5 show the nickel concentration in a silicon film obtained by introducing nickel using an aqueous acetate solution containing 100 ppm nickel and thereafter heat treating the silicon film at 550 °C for a duration of 4 hours. The nickel concentration is obtained by secondary ion mass spectroscopy (SIMS).

Fig. 4 shows the nickel concentration of the region 24 shown in Fig. 2C, i.e., the region into which nickel is directly incorporated. Fig. 5 shows the nickel concentration of the region 25 in Fig. 2C, i.e., the region in which crystal growth occurred along the lateral direction from the region 22.

By comparing the data of Fig. 4 with that of Fig. 5, it can be seen that the nickel concentration of the region in which the crystal growth occurs along the lateral direction is lower by about one digit as compared with that of the region into which nickel is introduced directly.

It can be seen also that the nickel concentration in the crystallized silicon film in the region into which nickel is introduced directly can be suppressed to a level of 10^{18} cm^{-3} by using an aqueous acetate solution containing nickel at a concentration of 10 ppm.

Conclusively, it is understood that the nickel concentration in the crystalline silicon region in which the crystal growth occurs along the lateral direction can be suppressed to 10^{17} cm^{-3} or lower by using an aqueous acetate solution containing nickel at a concentration of 10 ppm and effecting the heat treatment at 550 °C or higher for a duration of 4 hours or longer.

In conclusion, it is possible to control the concentration of nickel in the region 24 of the silicon film where the nickel is directly added within a range of 1 x 10^{16} atoms/cm^3 to 1 x 10^{19} atoms/cm^3 by controlling the density of the solution and the retention time and further to maintain the concentration of the nickel in the lateral growth region 25 below that.

For comparison, a sample is prepared through a process in which, instead of using a nickel containing solution, an amorphous silicon film is exposed to a plasma which is produced by using an electrode containing an amount of nickel in order to add the nickel into the silicon (this is called as a plasma treatment), and further the silicon film is crystallized by a heat annealing at 550 °C for 4 hours. The condition of the plasma treatment is selected so that the same degree of a lateral crystal growth can be obtained as in the case where an acetic acid containing nickel at 100 ppm is used. The SIMS data with respect to this sample is shown in Fig. 7. As can be seen, in the case of using a plasma treatment, the nickel concentration in the lateral growth region is higher than 5 x 10^{18} atoms/cm^3 which is undesirably high for an active region of a semiconductor device. Accordingly, it is to be understood that the use of a solution is advantageous for minimizing the concentration of the nickel in the lateral growth region.

Fig. 8 shows a result of Raman spectroscopy with respect to the region corresponding to Fig. 4, namely, the region where the nickel is directly introduced. Fig. 8 indicates that the crystallinity in this region is extremely high. Also, Fig. 9 shows a result of Raman spectroscopy with respect to the region where the crystal grows laterally. As can be seen, even in the lateral growth area, the intensity of the Raman spectrum is more than 1/3 of the intensity of the single crystal silicon. Accordingly, it is concluded that the crystallinity in the lateral growth region is also high.

The crystalline silicon film thus fabricated by the process according to the present invention is characterized in that it exhibits an excellent resistance against hydrofluoric acid. To the present inventors' knowledge, if the nickel is introduced by a plasma treatment, the resistivity of the crystallized silicon against a hydrofluoric acid is poor. When it is necessary to pattern a silicon oxide film which is formed over the crystalline silicon film for forming a contact hole therethrough, a hydrofluoric acid is usually used as an etchant. If the crystalline silicon film has a sufficiently high resistance against the hydrofluoric acid, a large selection ratio (the difference in the etching rate of the silicon oxide film and the crystalline silicon film) can be objected so as to remove the silicon oxide film alone. Accordingly, a crystalline silicon film having high resistance against attack of hydrofluoric acid is of great advantage in the fabrication process of a semiconductor device.

pressure CVD using TEOS together with ozone. The substrate temperature is maintained in the range of 250 to 450 °C, for instance, at 350 °C. A smooth surface is obtained thereafter by mechanically polishing the resulting silicon oxide film. An ITO coating is deposited thereon by sputtering, and is patterned to provide a pixel electrode 111 (Fig. 6D).

The interlayer dielectric 110 is etched to form contact holes in the source/drain as shown in Fig. 6E, and interconnections 112 and 113 are formed using chromium or titanium nitride to connect the interconnection 113 to the pixel electrode 111.

In the process according to the present invention, nickel is incorporated into the silicon film by using an aqueous solution containing nickel at such a low concentration of 10 ppm. Accordingly, a silicon film having a high resistance against hydrofluoric acid can be realized and contact holes can be formed stably and with high reproducibility.

A complete TFT can be formed by finally annealing the silicon film in hydrogen in a temperature range of 300 to 400 °C for a duration of from 0.1 to 2 hours to accomplish the hydrogenation of the silicon film. A plurality of TFTs similar to the one described hereinbefore are fabricated simultaneously, and are arranged in a matrix to form an active matrix liquid crystal display device.

In accordance with the present example, the concentration of the nickel contained in the active layer is in the range of 5×10^{16} to 3×10^{18} atoms/cm^3.

As described above, the process according to the present example comprises crystallizing the portion into which nickel is introduced. However, the process can be modified as in Example 2. That is, nickel can be incorporated to selected portions through a mask, and crystals may be allowed to grow from the portions in a lateral direction. This region of crystal growth is used for the device. A device far more preferred from the viewpoint of electric stability and reliability can be realized by further lowering the nickel concentration of the active layer region of the device.

[Example 4]

This example is directed to a manufacture of a TFT used to control a pixel of an active matrix. Figs. 10A-10F are cross sectional views for explaining the manufacture of the TFT in accordance with this example.

Referring to Fig. 10A, a substrate 201, for example glass substrate, is washed and provided with a silicon oxide film 202 on its surface. The silicon oxide film 202 is formed through a plasma CVD with oxygen and tetraethoxysilane used as starting gases. The thickness of the film is 2000 Å, for example. Then, an amorphous silicon film 203 of an intrinsic type having a thickness of 500 - 1500 Å, for example, 1000 Å is formed on the silicon oxide film 202, following which a silicon oxide film 205 of 500 - 2000 Å, for example 1000 Å is formed on the amorphous silicon film successively. Further, the silicon oxide film 205 is selectively etched in order to form an opening 206 at which the amorphous silicon film is exposed.

Then, a nickel containing solution (an acetic acid salt solution here) is coated on the entire surface in the same manner as set forth in Example 2. The concentration of nickel in the acetic acid salt solution is 100 ppm. The other conditions are the same as in Example 2. Thus, a nickel containing film 207 is formed.

The amorphous silicon film 203 provided with the nickel containing film in contact therewith is crystallized through a heat annealing at 500 - 620 °C for 4 hours in a nitrogen atmosphere. The crystallization starts from the region under the opening 206 where the silicon film directly contacts the nickel containing film and further proceeds in a direction parallel with the substrate. In the figure, a reference numeral 204 indicates a portion of the silicon film where the silicon film is directly added with nickel and crystallized while a reference numeral 203 indicates a portion where the crystal grows in a lateral direction. The crystals grown in the lateral direction are about 25 µm. Also, the direction of the crystal growth is approximately along an axes of [111].

After the crystallization, the silicon oxide film 205 is removed. At this time, an oxide film formed on the silicon film in the opening 206 is simultaneously removed. Further, the silicon film 204 is patterned by dry etching to form an active layer 208 in the form of an island as shown in Fig. 10B. It should be noted that the nickel is contained in the silicon film at a higher concentration not only under the opening 206 where the nickel is directly added but also at a portion where top ends of the crystals exist. The patterning of the silicon film should be done in such a manner that the patterned silicon film 208 should not include such portions at which nickel is contained at a higher concentration.

The patterned active layer 208 is then exposed to an atmosphere containing 100 % aqueous vapor of 10 atm at 500 - 600 °C, typically, 550 °C for one hour in order to oxidize the surface thereof and thus to form a silicon oxide film 209 of 1000 Å. After the oxidation, the substrate is maintained in an ammonium atmosphere (1 atm, 100 %) at 400 °C. At this condition, the silicon oxide film 209 is irradiated with an infrared light having an intensity peak at a wavelength in the range of 0.6 - 4 µm, for example, 0.8 - 1.4 µm for 30 - 180 seconds in order to nitride the silicon oxide film 209. HCl may be added to the atmosphere at 0.1 to 10 %. A halogen lamp is used as a light source of the infrared light. The intensity of the IR light is controlled so that a temperature on the surface of a monitoring single crystalline silicon wafer is set between 900 - 1200 °C. More specifically, the temperature is monitored by means of a thermocouple embedded in a sin-

the surface of the silicon film is reduced (eaten) by 50 Å or more due to the oxidation, an effect of a contamination of the upper most surface of the silicon film does not extend to the silicon-silicon oxide interface. In other words, by the oxidation, it is possible to obtain a clean silicon-silicon oxide interface. Also, since the thickness of the silicon oxide film is two times as the thickness of the portion of the silicon film to be oxidized, when the silicon film is originally 1000 Å thick and the silicon oxide film obtained is 1000 Å, the thickness of the silicon film remaining after the oxidation is 500 Å.

Generally, the thinner a silicon oxide film (gate insulating film) and an active layer are, the higher a mobility is and the smaller an off current is. On the other hand, a preliminary crystallization of an amorphous silicon film is easier when its thickness is thicker. Accordingly, there was a contradiction in the crystallization process and electrical characteristics with respect to the thickness of the active layer. The present example advantageously solves this problem. That is, the amorphous silicon film having a larger thickness is initially formed so that a better crystalline silicon film can be obtained, following which the thickness of the silicon film is reduced by the oxidation, resulting in an improvement of characteristics of the active layer of a TFT. Moreover, an amorphous component or grain boundaries contained in the crystalline silicon film tend to be oxidized during the thermal oxidation, resulting in a decrease in recombination centers contained the active layer.

After the formation of the silicon oxide film 209 through thermal oxidation, the substrate is annealed in a 100 % monoxide dinitrogen atmosphere at 1 atm and 600 °C for 2 hours.

Referring to Fig. 11C, a silicon containing 0.01 to 0.2 % phosphorous is deposited through low pressure CVD to 3000 - 8000 Å thick, for example, 6000 Å, and then patterned into a gate electrode 210. Further, using the gate electrode 210 as a mask, an N-type conductivity impurity is added into a portion of the active layer in a self-aligning manner by ion doping. Phosphine is used as a dopant gas. The doping condition is substantially the same as in the Example 4. The dose amount is, for example, 5×10^{15} cm^{-2}. Thus, N-type impurity regions 212 and 213 are formed.

Thereafter, an annealing is performed with a KrF excimer laser in the same manner as set forth in Example 4. The laser annealing may be replaced by a lamp annealing with a near infrared ray. The near infrared ray is absorbed by crystalline silicon more effectively than by amorphous silicon. Accordingly, the annealing with the near infrared ray is comparable with a thermal annealing at 1000 °C or more. On the other hand, it is possible to prevent the glass substrate from being detrimentally heated inasmuch as the near infrared ray is not so absorbed by the glass substrate. That is, although a far infrared ray can be absorbed by a glass substrate, visible or near infrared ray of which wavelength ranges from 0.5 - 4 μm are not so absorbed.

Referring to Fig. 11D, an interlayer insulating film 214 of silicon oxide is formed to 6000 Å thick by a plasma CVD. A polyimide may be used instead of silicon oxide. Further, contact holes are formed through the insulating film. Electrode/wirings 217 and 218 are formed through the contact holes by using a multilayer of titanium nitride and aluminum films. Finally, an annealing in a hydrogen atmosphere is conducted at 350 °C and 1 atm for 30 minutes. Thus, a TFT is completed.

The mobility of the thus formed TFT is 110 - 150 cm^2/Vs. The S value is 0.2 - 0.5 V/digit. Also, in the case of forming a P-channel type TFT by doping boron into source and drain regions, the mobility is 90 - 120 cm^2/Vs and the S value is 0.4 - 0.6 V/digit. The mobility in accordance with the present example can be increased by 20 % or more and the S value can be reduced by 20 % or more as compared with a case where a gate insulating film is formed by a known PVD or CVD.

Also, the reliability of the TFT in accordance with the present example is comparable to that of a TFT which is produced through a thermal oxidation at a temperature as high as 1000 °C.

[Example 6]

Fig. 12 shows an example of an active matrix type liquid crystal device in accordance with the present example.

In the figure, reference numeral 61 shows a glass substrate, and 63 shows a pixel area having a plurality of pixels in the form of a matrix each of which is provided with a TFT as a switching element. Reference numeral 62 shows peripheral driver region(s) in which driver TFTs are provided in order to drive the TFTs of the pixel area. The pixel area 63 and the driver region 62 are united on the same substrate 61.

The TFTs provided in the driver region 62 need to have a high mobility in order to allow a large amount of electric currents to pass therethrough. Also the TFTs provided in the pixel area 63 need to have a lower leak current property in order to increase a charge retention ability of pixel electrodes. For example, the TFTs manufactured in accordance with Example 3 are suitable as the TFTs of the pixel area 63.

[Example 7]

The present example is a modification of Example 1. That is, before forming a nickel acetate aqueous solution, a rubbing treatment is performed on a silicon oxide surface in order to form number of minute scratches there.

Referring to Fig. 13A, a Corning 7059 substrate

the width of the grains 19 are approximately constant and the number of grains existing in the channel region 26 can be made constant. In conclusion, it is desirable to arrange the active region 208 in such a way that a drain current of a TFT flows in a direction perpendicular to the direction of grain boundaries, i.e. the rubbing directions. Moreover, the rubbing treatment makes the size of crystal grains uniform, which results in that non-crystallized region can be epitaxially crystallized by a subsequent laser irradiation.

As shown in Fig. 14B, a silicon oxide film of 200 - 1500 Å thick, for example, 1000 Å thick is formed as a gate insulating film 209 through plasma CVD.

Then, an aluminum containing Si at 1 weight % or Sc at 0.1 to 0.3 weight % is sputter formed to 1000 Å to 3 μm, for example 5000 Å, following which it is patterned into a gate electrode 210. The aluminum electrode is then subjected to an anodic oxidation process using an ethylene glycol solution containing a tartaric acid at 1-3 %. The pH of the electrolyte is about 7. A platinum electrode is used as a cathode while the aluminum electrode is used as an anode. The voltage is increased with an electric current maintained constant until it reaches 220 V and then this condition is maintained for one hour. As a result, an anodic oxide film 211 is formed to a thickness of 1500 - 3500 Å, for example 2000 Å.

Referring to Fig. 14C, an impurity having one conductivity type (boron) is introduced into the silicon island through an ion doping method with the gate electrode 210 used as a mask in a self-aligning manner. Diborane (B_2H_6) is used as a dopant gas. The dose amount is 4-10 x 10^{15} cm^{-2}. The acceleration voltage is 65 kV. Thus, a pair of impurity regions (p-type) 212 and 213 are obtained.

Thereafter, the impurity regions 212 and 213 are activated by irradiating KrF excimer laser (248 nm wavelength, 20 nsec. pulse width). The energy density of the laser beam is 200 - 400 mJ/cm^2, preferably, 250 - 300 mJ/cm^2.

Referring to Fig. 14D, an interlayer insulating film 214 made of silicon oxide is formed through plasma CVD to a thickness of 3000 Å. Then, a contact hole is formed on the impurity region 212 (source) through the interlayer insulating film 214 and the gate insulating film 209 by etching. An aluminum film is then formed by sputtering and patterned to form a source electrode 217.

Referring to Fig. 14E, silicon nitride is deposited through plasma CVD to 2000 - 6000 Å as a passivation film 215. A contact hole is formed on the impurity region (drain) 213 through the passivation film 215, interlayer insulating film 214 and the gate insulating film 209 by etching. Finally, an indium tin oxide film (ITO) is formed into a pixel electrode 216. Thus, a pixel TFT is obtained.

While the present invention has been disclosed in preferred embodiments, it is to be understood that the scope of the present invention should not be limited to the specific examples of the embodiments. Various modifications may be made.

For example, the nickel containing film may be formed by using a non-aqueous solution such as alcohol. When using an alcohol, the solution may be directly formed on the amorphous silicon film without using an oxide film. Specifically, a nickel containing compound such as nickel acetyl acetonate may be dissolved by ethanol. This material can be decomposed during the heating for the crystallization because the decomposition temperature thereof is relatively low. The amount of the nickel acetyl acetonate is selected so that the concentration of the nickel in the solution is controlled to be 100 ppm. The nickel containing film can be obtained by coating the solution and then dried by a spin dry method at 1500 rpm for 1 minute. Also, since the contact angle of the alcohol is smaller than that of water, the amount of the solution used for forming the film may be smaller than in the case when a water solution is used. In this case, a drop of 2 ml with respect to 100 mm square is appropriate. The subsequent steps for forming the crystalline silicon may be entirely the same as those explained in the preferred embodiments.

For another example, an elemental nickel may be dissolved by an acid. That is, a nitric acid of 0.1 mol/l is used as an acid. Nickel powder is dissolved in this acid at 50 ppm.

Claims

1. A method for manufacturing a semiconductor device comprising the steps of:
   disposing a solution in contact with a portion of a silicon film on a substrate, said solution containing a catalyst for promoting a crystallization of said silicon film; and
   crystallizing said silicon film by heating.

2. The method of claim 1 wherein said catalyst comprises a material selected from the group consisting of nickel (Ni), palladium (Pd), platinum (Pt), copper (Cu), silver (Ag), gold (Au), indium (In), tin (Sn), phosphorus (P), arsenic (As), and antimony (Sb).

3. The method of claim 1 wherein said catalyst is included in said solution at a concentration from 200 ppm or lower.

4. The method of claim 1 wherein concentration of the catalyst in the solution is 50 ppm or lower.

5. The process of claim 1 wherein concentration of the catalyst in the solution is 10 ppm or lower.

silicon film; and then

crystallizing said silicon film by heating.

26. The method of claim 25 wherein said polar solvent is selected from the group consisting of water, alcohol, acid and ammonium.

27. The method of claim 25 wherein said compound is selected from the group consisting of nickel bromide, nickel acetate, nickel oxalate, nickel carbonate, nickel chloride, nickel iodide, nickel nitrate, nickel sulfate, nickel formate, nickel acetyl acetonate, 4-cyclohexyl butyric acid, nickel oxide and nickel hydroxide.

28. The method of claim 25 further comprising the step of adding an interfacial active agent.

29. The method of claim 25 further comprising the step of interposing an oxide film between said solution and said silicon film.

30. A method for manufacturing a semiconductor device comprising the steps of:

preparing a solution containing a compound dissolved or dispersed in a non-polar solvent, said compound including a crystallization promoting material;

disposing said solution in contact with a silicon film; and then

crystallizing said silicon film by heating.

31. The method of claim 30 wherein said non-polar solvent is selected from the group consisting of benzene, toluene, xylene, carbon tetrachloride, chloroform and ether.

32. The method of claim 30 wherein said compound is selected from the group consisting of nickel acetyl acetonate, 2-ethyl hexanoic acid nickel, nickel bromide, 4-cyclohexyl butyric acid, nickel oxide and nickel hydroxide.

33. A method for manufacturing an insulated gate field effect semiconductor device comprising the steps of:

forming an amorphous silicon film on an insulating surface;

crystallizing said silicon film; and

oxidizing a surface of said silicon film in an oxidizing atmosphere containing water vapor in order to form a gate insulating film.

34. The method of claim 33 further comprising the step of adding nickel into said amorphous silicon film before said crystallizing.

35. The method of claim 33 further comprising treating said silicon film in a nitrogen containing atmosphere with light after said oxidizing.

36. A semiconductor device including at least an active region comprising crystalline silicon formed on an insulating surface, wherein said silicon film contains a catalyst element which promotes a crystallization of an amorphous silicon film.

37. The device of claim 36 wherein said catalyst element comprises a material selected from the group consisting of nickel (Ni), palladium (Pd), platinum (Pt), copper (Cu), silver (Ag), gold (Au), indium (In), tin (Sn), phosphorus (P), arsenic (As), and antimony (Sb).

38. The device of claim 36 wherein said device is selected from the group consisting of a thin film transistor, diode and photosensor.

39. The device of claim 36 wherein said device includes at least one electric junction indicated by PI, PN and NI.

40. The device of claim 36 wherein said catalyst element is contained in said silicon film at a concentration in the range of 1×10^{16} atoms/cm^3 to 1×10^{19} atoms/cm^3.

41. The device of claim 36 wherein a peak intensity of a Raman spectroscopy with respect to said silicon film is 1/3 or more than a peak intensity of a Raman spectroscopy with respect to a single crystal silicon.

42. The device of claim 36 wherein a crystal growth direction of said silicon film is approximately aligned with [111] axes.

43. The device of claim 36 wherein a surface of said silicon film has at least one of planes {111}, those expressed by {hkl} (h+k=l), and a neighborhood thereof.

44. The device of claim 43 wherein the planes expressed by {hkl} are {110}, {123}, {134}, {235}, {145}, {156}, {257}, and {167}.

45. A semiconductor device including at least an active region comprising crystalline silicon formed on a substrate, wherein a surface of said silicon film has at least one of planes {111}, those expressed by {hkl} (h+k=l), and a neighborhood thereof.

46. The device of claim 45 wherein the planes expressed by {hkl} are {110}, {123}, {134}, {235}, {145}, {156}, {257}, and {167}.

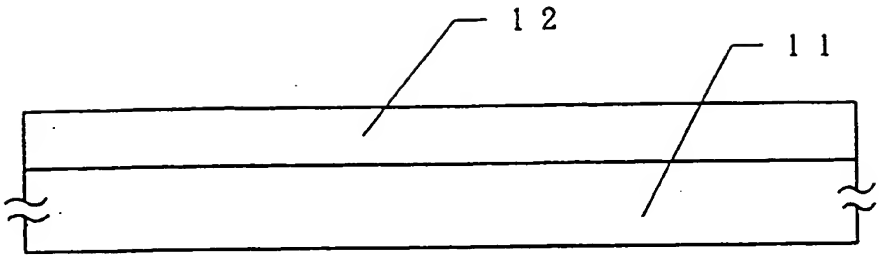


Fig.1A

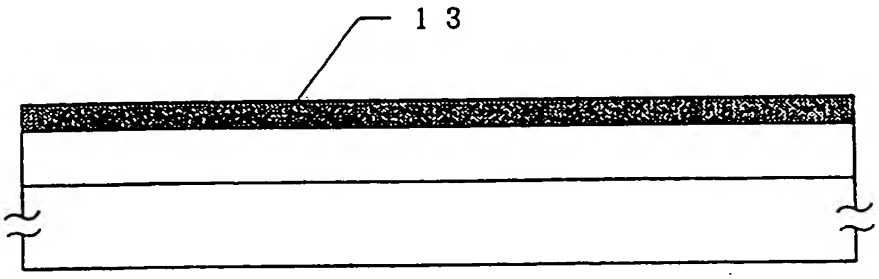


Fig.1B

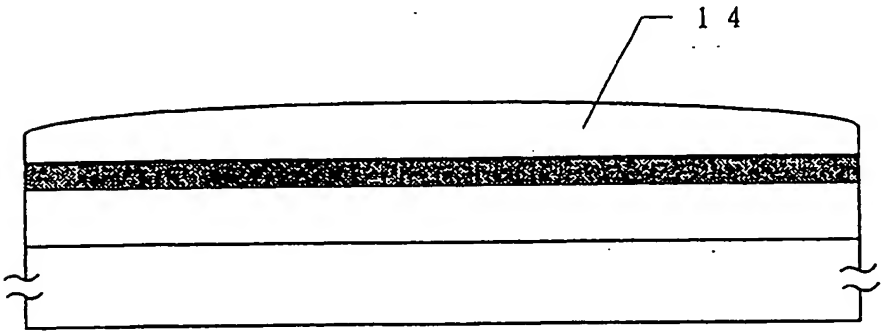


Fig.1C

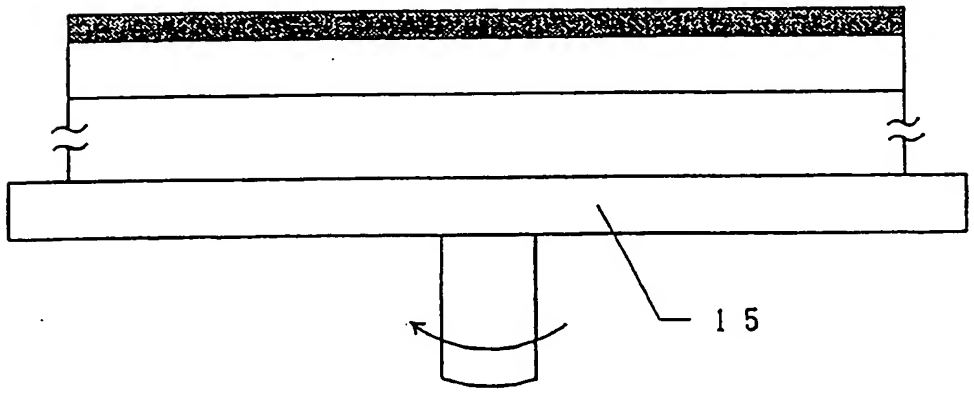


Fig.1D

Fig. 3

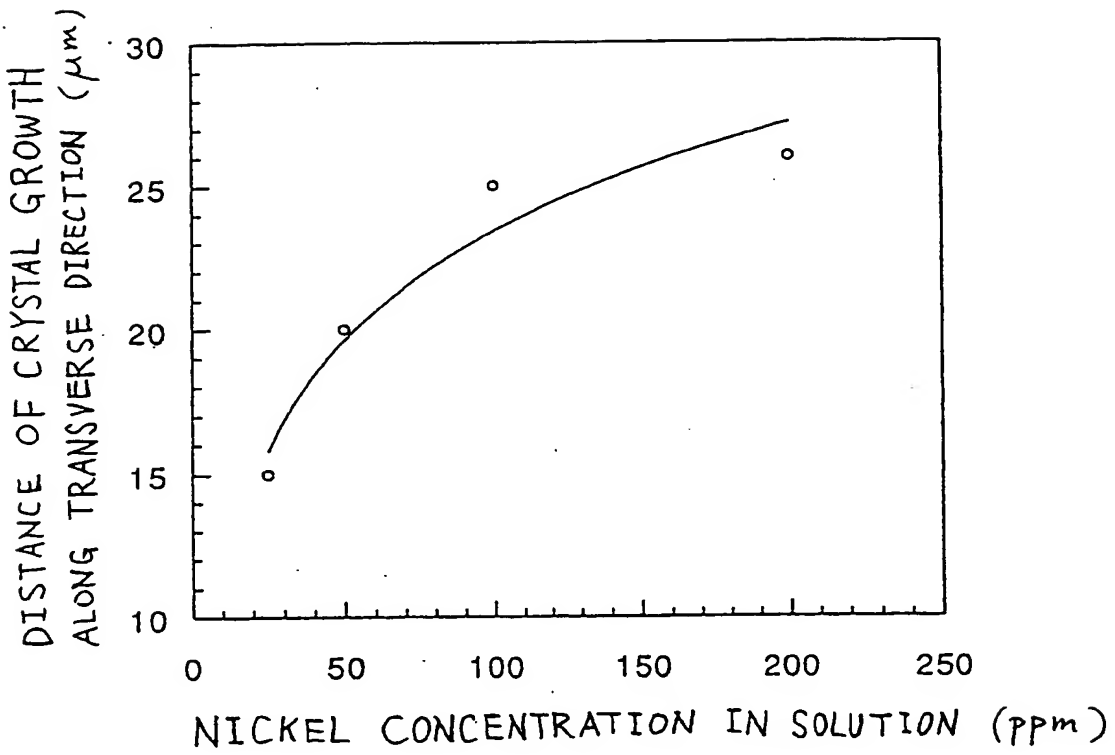
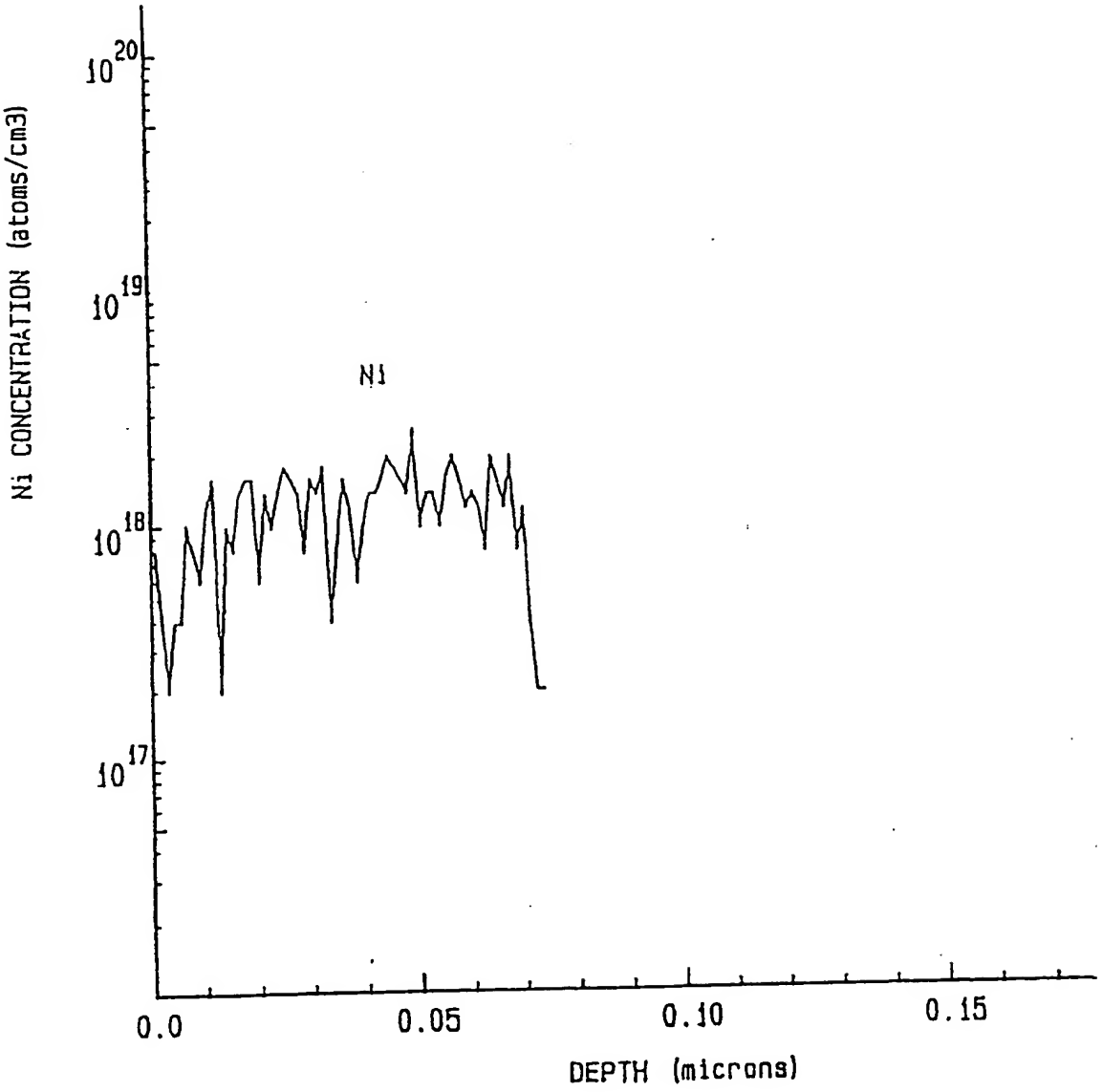


Fig. 5



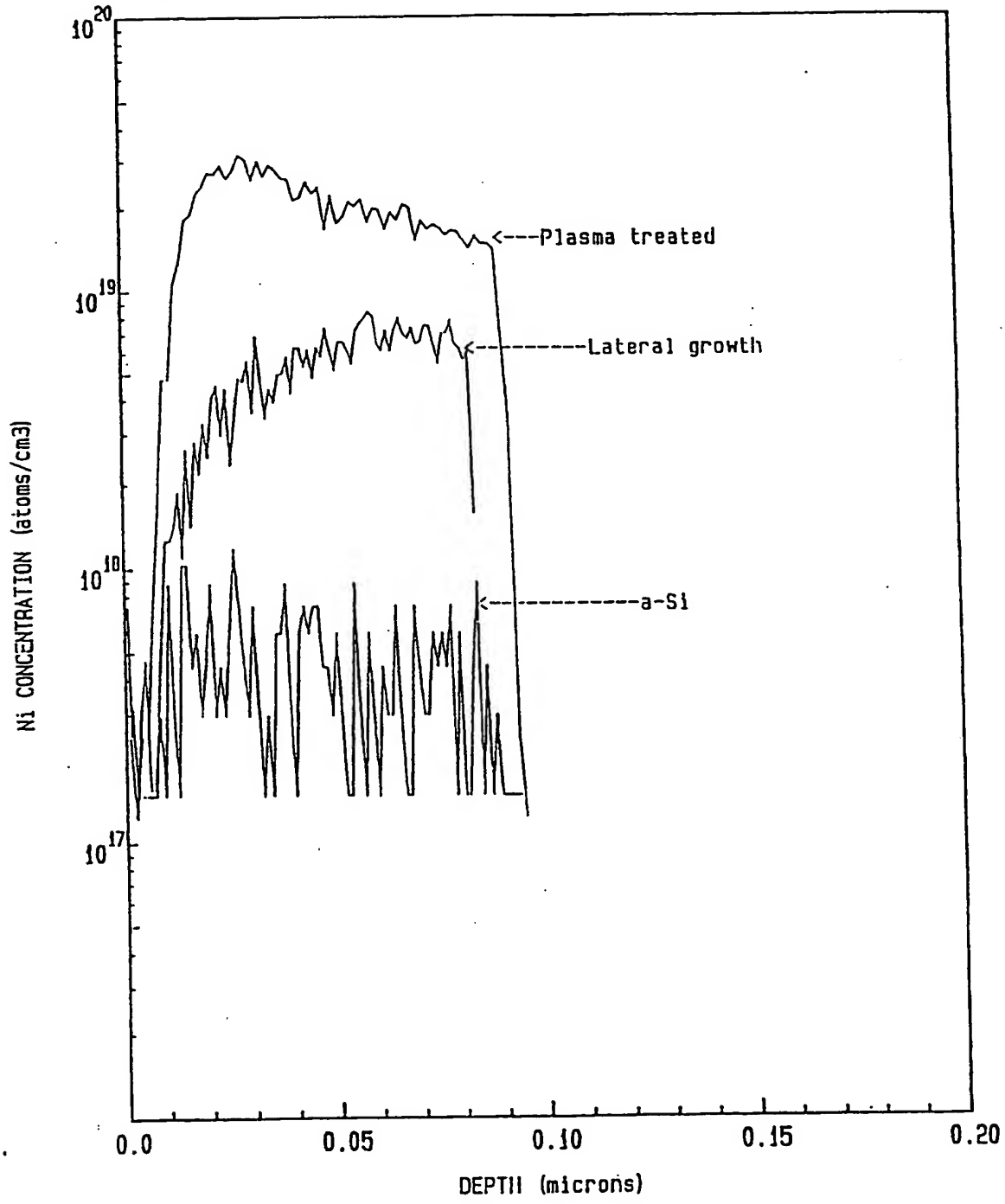


Fig. 7

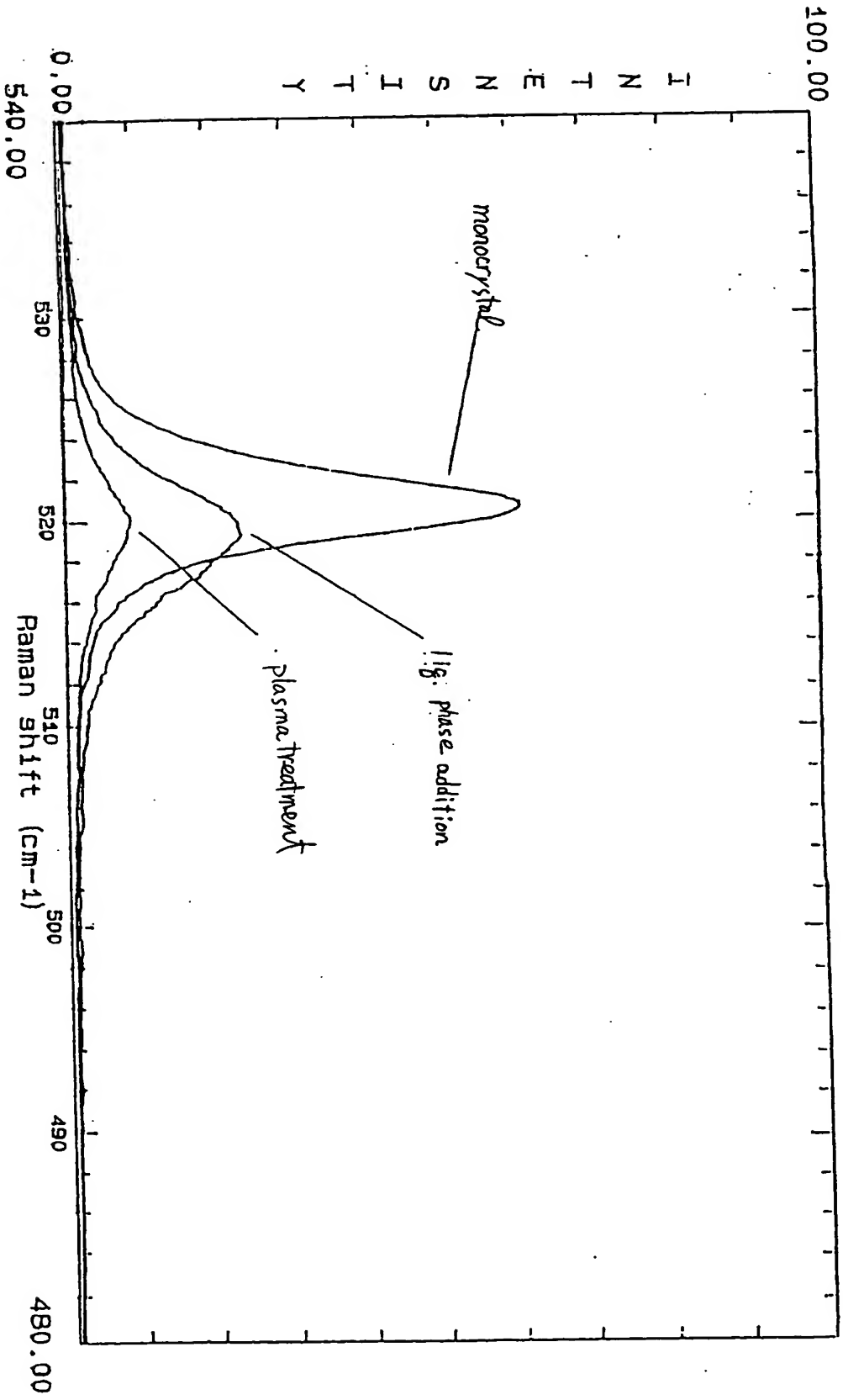


Fig. 9

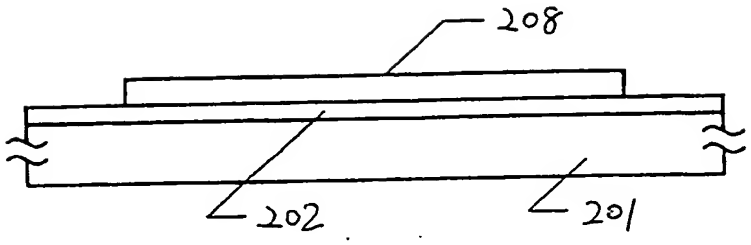


Fig. 11A

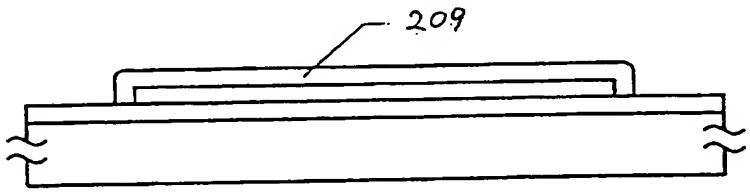


Fig. 11B

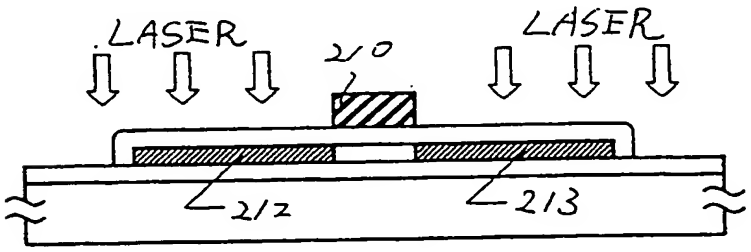


Fig. 11C

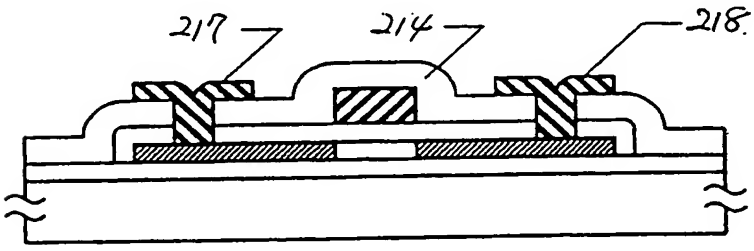


Fig. 11D

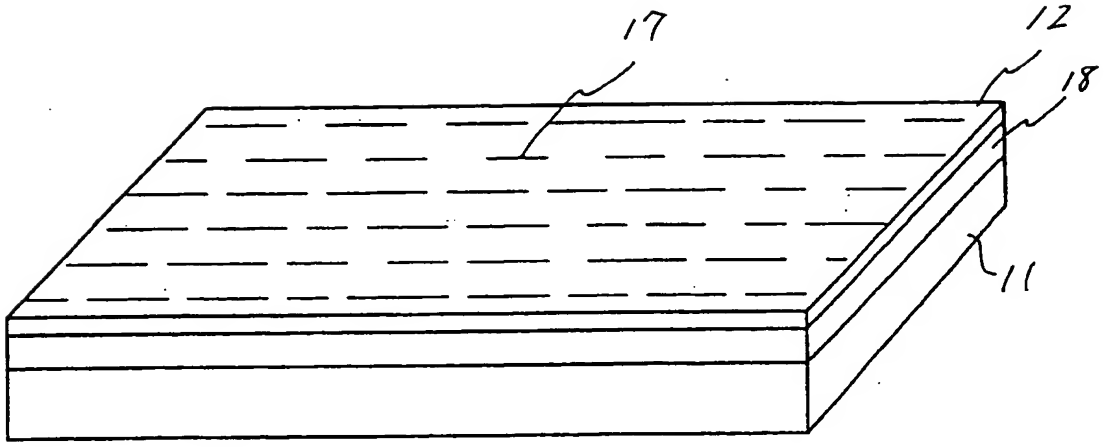


Fig. 13A

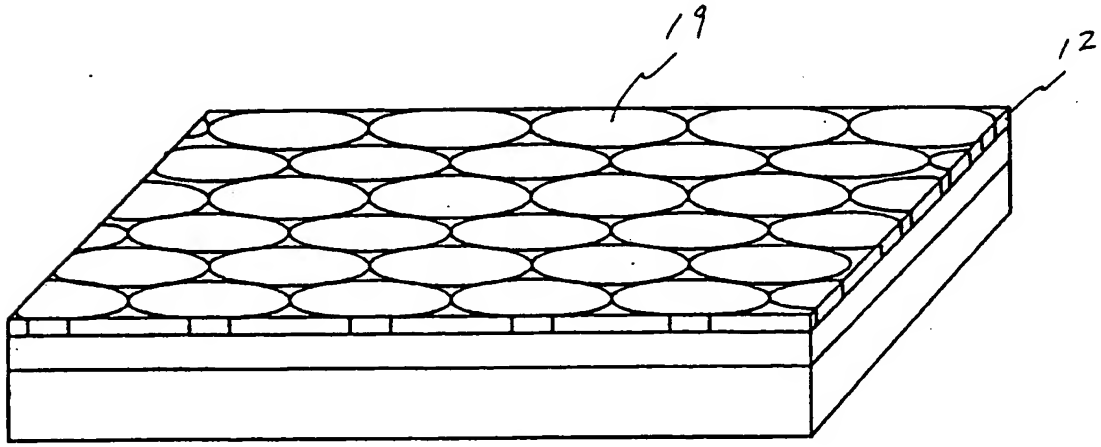


Fig. 13 B

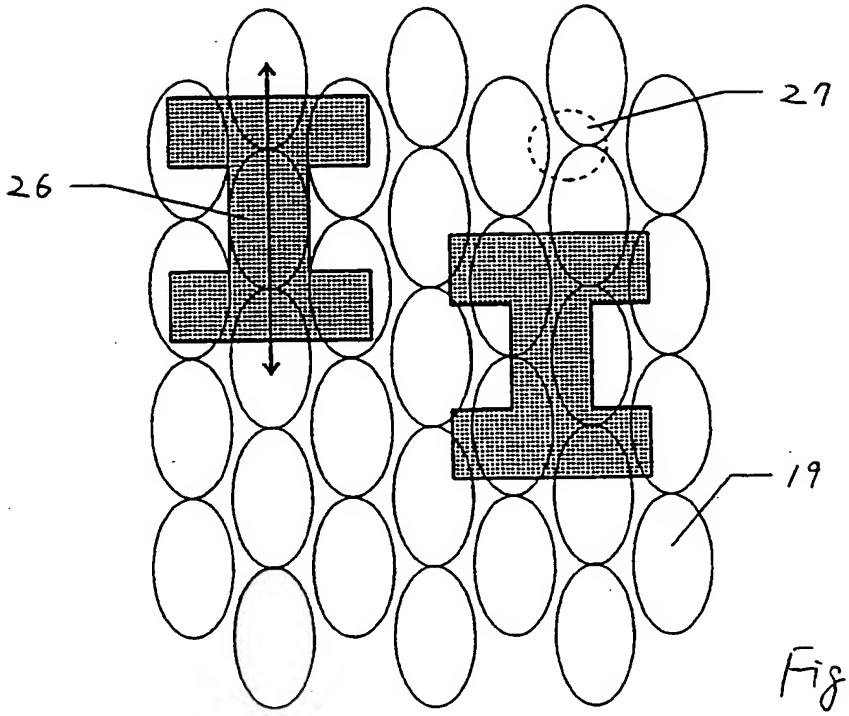


Fig. 15A

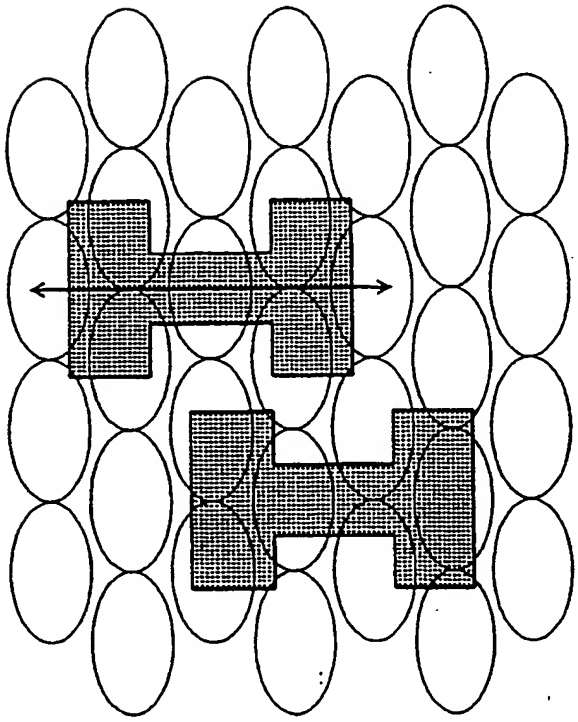


Fig. 15B

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 651 431 A3**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **94307986.3**

(51) Int. Cl.[6] : **H01L 21/20**, H01L 21/336

(22) Date of filing : **31.10.94**

(30) Priority : **29.10.93 JP 294633/93**
09.11.93 JP 303436/93
12.11.93 JP 307206/93
20.06.94 JP 162705/94

(43) Date of publication of application :
03.05.95 Bulletin 95/18

(84) Designated Contracting States :
DE FR GB NL

(88) Date of deferred publication of search report :
07.06.95 Bulletin 95/23

(71) Applicant : **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.**
398 Hase
Atsugi-shi Kanagawa-ken, 243 (JP)

(72) Inventor : **Ohtani, Hisashi**
Mac Aikoishida Court,
501 7-896-1, Takamori
Isehara-shi, Kanagawa-ken 259-11 (JP)
Inventor : **Miyanaga, Akiharu**
2-505, 3-4-1, Minamigaoka
Hadano-shi, Kanagawa-ken 257 (JP)
Inventor : **Fukunaga, Takeshi**
Flat SEL-A 105,
304-1, Hase
Atsugi-shi, Kanagawa-ken 243 (JP)
Inventor : **Zhang, Hongyong**
Paresu Miyagami 302,
1-10-15, Fukamidai
Yamato-shi, Kanagawa-ken 243 (JP)

(74) Representative : **Milhench, Howard Leslie et al**
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

(54) Method of crystallizing a silicone layer and semiconductor devices obtained by using the method.

(57) A process for fabricating a highly stable and reliable semiconductor, comprising : coating the surface of an amorphous silicon film with a solution containing a catalyst element capable of accelerating the crystallization of the amorphous silicon film, and heat treating the amorphous silicon film thereafter to crystallize the film.

EP 0 651 431 A3

European Patent Office

EP 94307986.3

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions.

namely:

See Sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☒ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.

namely claims: 33-35

☐ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

namely claims: